REMARKS

Reconsideration of the present application is respectfully requested. In this amendment, claims 1, 7 and 8 have been amended. No claims have been canceled or added. No new matter has been added.

Claim 7 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 15, 16, 19, 20, 23, 24, 26, 29 and 32 stand rejected under 35 U.S.C. § 102(e) based on U.S. Patent no. 6,534,726 of Okada et al. ("Okada"). Claims 8, 12-14, 17 and 27 stand rejected under 35 U.S.C. § 103(a) based on Okada. Claims 1, 5, 6, 9-11, 21, 22, 25, 28, 30 and 31stand rejected under 35 U.S.C. § 103(a) based on Okada in view of U.S. Patent no. 5,222,014 of Lin et al. ("Lin").

The present application includes four independent claims, i.e., claims 1, 8, 15 and 23.

Claim 1

Claim 1, as amended, recites:

> 1. (Currently amended) A method comprising:
> (a) creating a plurality of rows of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate, the plurality of rows all being defined parallel to a coordinate axis;
> (b) forming a conductive layer on the first surface and on the second surface;
> (c) forming a conductive path through each of the via holes from the first surface to the second surface;
> (d) severing the substrate through each of the plurality of rows of via holes and between each of the plurality of rows of via holes along a coordinate axis, to produce a plurality of elongate substrate members, each of the elongate substrate members having a first surface formed from a portion of the first surface of the circuit board substrate; and
> (e) affixing together two or more elongate substrate members

created as recited in said (a), (b), (c) and (d), **to form an interposer with a plurality of conductive vias arranged in a two-dimensional array, the array being defined substantially in a plane parallel to the first surfaces of the elongate substrate members.**
(Emphasis added.)

Applicants have amended claim 1 to clarify what was meant by "edgewise orientation" (this phrase has now been deleted) in the previous version of claim 1. As such, Okada and Lin do not disclose or suggest, either individually or in combination, affixing together two or more of elongate substrate members, created as recited in the claim, to form an interposer with a plurality of conductive vias arranged in a two-dimensional array, the array being defined substantially in a plane parallel to the first surfaces of the elongate substrate members. An example of this is shown in Figure 7 of the present application, in which the "first surfaces" of the elongate substrate members are parallel to the page.

The Examiner admits that "Okada does not appear to explicitly disclose elongate substrate members" (Final Office Action, p. 12). However, the Examiner contends that the claimed invention feature would be obvious in view of Lin, particularly Lin's disclosure at col. 3, lines 1-26; col. 3 line 58 to col. 2 line 59; col. 5, lines 29-31 and col. 6 lines 22-59 (Office Action, p. 13). Applicants respectfully disagree.

Okada discloses a technique for producing a module substrate onto which an electronic component can be mounted, and which can be mounted to a motherboard. The substrate includes a number of through holes that can be filled with a conductive material. Lin, on the other hand, discloses a multi-chip module (MCM), the different layers of which are stacked over each other. For example, in Fig. 1 of Lin, semiconductor die 10 is sandwiched vertically between substrates 12 and 20.

Assuming *arguendo* the teachings of Okada and Lin can even be combined, at best such combination would suggest stacking Okada's substrates on top of each other. Such a configuration would be contrary to the language of claim 1, which requires that the conductive vias be arranged in a two-dimensional array, where the array is defined substantially in a plane parallel to the first surfaces of the elongate substrate members, which to facilitate discussion can be called a "horizontal" array. At best, a stacked configuration per Okada/Lin might create a substantially vertical array of conductive vias, where the array is not substantially in any plane parallel to the first surfaces of the elongate substrate members. There is absolutely no teaching or suggestion in Okada or Lin, individually or in combination, to affix together two or more elongate substrate members, constructed as recited in claim 1, in a configuration as recited in claim 1.

Furthermore, there is no suggestion in either Okada or Lin as to why such a configuration would even be desirable. Note that the affixing operation, as recited in claim 1, is done specifically for the purpose of forming a two-dimensional array of vias. In contrast, the stacking of layers in Lin is done to conserve space on the motherboard (see Lin at col. 3, lines 58-62).

The Examiner states (Final Office Action, p. 12):

> Notwithstanding [that Okada does not disclose elongate beams], it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular shape because applicant has not disclosed that, in view of the applied prior art, the shape is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical.

Applicants respectfully submit that the Examiner is clearly mistaken in the above contention. First, whether or not the claim invention would be an "obvious matter of

design choice" does not depend on what Applicant has disclosed or not disclosed (as the above quote implies), since obviousness is not evaluated based on the sufficiency or depth of an applicant's disclosure. Furthermore, Applicants clearly have described in abundant detail (in their specification, in the previous responses, and above in this response) that the "shape" is indeed for particular unobvious purpose or is otherwise critical. The claimed configuration is clearly not an obvious matter of design choice.

Therefore, the invention as set forth in claim 1 is not obvious based on Okada, Lin, or any combination thereof.

Claim 8

Claim 1 stands rejected under 35 U.S.C. § 103(a) based on Okada. Claim 8 provides:

> 8. (Currently amended) A method of manufacturing an interposer, the method comprising:
> creating a plurality of rows of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate, the first surface and the second surface being coated with a conductive material;
> forming a conductive layer in each of the via holes to provide a conduction path through each of the via holes from the conductive material on the first surface to the conductive material on the second surface;
> selectively removing some of the conductive material from the first surface and the second surface to form a plurality of traces on the first surface and the second surface, each trace in electrical contact with the conductive layer in at least one of the via holes; and
> severing the substrate to produce a plurality of individual substrate members, by cutting the substrate through the middle of the via holes in each row of via holes **and between every pair of adjacent rows of via holes** along a particular axis.
> (Emphasis added).

Neither Okada nor Lin discloses or suggests severing the substrate to produce a plurality of individual substrate members, by cutting the substrate through the middle of the via holes in each row of via holes and between every pair of adjacent rows of via holes along a particular axis. This manner of severing results in the creation of elongate members and facilitates the subsequent affixing of the elongate members together to form a two-dimensional array of contacts (although the affixing operation is not recited in claim 8).

It is noted that Okada discloses severing the substrate through the middle of a row of through holes (see Fig. 9), but not between every pair of adjacent rows of through holes along a particular axis. Furthermore, Okada provides no motivation as to why it would be desirable to do so; in fact, it is not even apparent how that would be possible in Okada, given the shape and configuration of the substrates 11, 21 in Okada. Likewise, Lin also does not suggest the manner of severing a substrate as recited in claim 8.

Furthermore, the Examiner states (Final Office Action, p. 10):

> Notwithstanding [that Okada does not disclose elongate beams], it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular shape because applicant has not disclosed that, in view of the applied prior art, the shape is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical.

Applicants respectfully submit that the Examiner is clearly mistaken in the above contention. First, whether or not the claim invention would be an "obvious matter of design choice" does not depend on what Applicant has disclosed or not disclosed, as the above quote implies, since obviousness is not evaluated based on the sufficiency or

depth of an applicant's disclosure. Furthermore, Applicants clearly have described in abundant detail (in their specification, in the previous responses, and above in this response) that the "shape" is indeed for particular unobvious purpose or is otherwise critical. The claimed configuration is clearly not an obvious matter of design choice.

Therefore, the invention as set forth in claim 8 is not obvious based on Okada, Lin, or any combination thereof.

Claim 15

Claim 15 stands rejected under 35 U.S.C. § 102(e) based on Okada. Claim 15, as amended, provides:

> 15. (Previously presented) A method of manufacturing an interposer, the method comprising:
> creating a plurality of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate;
> creating a solid conductive column through each of the via holes, the conductive column forming an electrical path from the first surface to the second surface; and
> **forming grooves** in the first surface and the second surface of the substrate **between the via holes.**
> (Emphasis added.)

Okada does not disclose or suggest such a method. In particular, Okada does not disclose or suggest forming grooves in the first surface and the second surface of the substrate between the via holes. On p. 5 of the Final Office Action the Examiner contends that Okada discloses such an operation as "forming grooves 53 in the first surface and the second surface between the via holes." On page 6 of the Final Office Action, the Examiner clarifies his interpretation as follows:

> To further clarify the disclosure of forming grooves 53 in the first surface and the second surface of the substrate, the end portions of the

grooves (illustrated but not labeled) are formed in the first and second surface of the substrate.

Applicant respectfully submits that the Examiner's interpretation is both incorrect and unreasonable. No one who has even a marginal understanding of English could reasonably consider the grooves 53 in Okada (see Fig. 16) to be formed "in" the first and second surfaces 51A and 51B of the substrate. To the contrary, the grooves 53 in Okada are formed "between" the first surface 51A and the second surface 51B; or stated another way, they are formed "from" the first surface 51A "to" the second surface 51B. That is different from being formed "in" the first and second surfaces.

The grooves 53 in Okada are defined "in" the end faces 51C (col. 11, lines 16-18). The end faces 51C clearly cannot be read on the first or second surfaces of claim 15. Claim 15 requires that the via holes are formed from the first surface to the second surface, but that the grooves are formed in the first and second surfaces. To read Okada on claim 15, therefore, the first and second surfaces would have to be the front surface 51A and back surface 51B of the substrate 51 (referring, for example, to Fig. 16 of Okada). However, such a reading defies the claim language, as explained above. Therefore, Okada fails to read on claim 15.

Applicants respectfully submits that claims cannot be given an interpretation during examination which is unreasonable in light of both the Applicant's disclosure and the ordinary meaning of the claim language. Therefore, the invention as set forth in claim 8 is not anticipated or obvious based on Okada.

Claim 23

Claim 23 includes limitations substantially similar to those discussed above with regard to claim 15. Therefore, claim 23 is also patentably distinguishable from the cited art for essentially the same reasons as claim 15.

Dependent Claims

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

Conclusion

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,
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